

FIG. 1

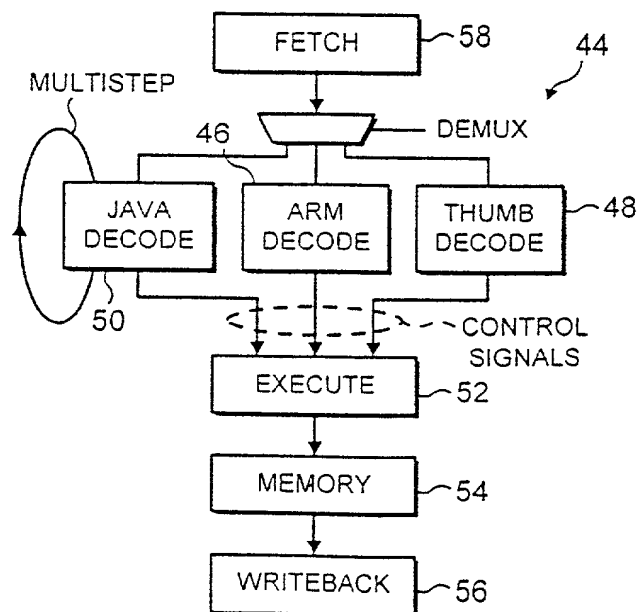


FIG. 2

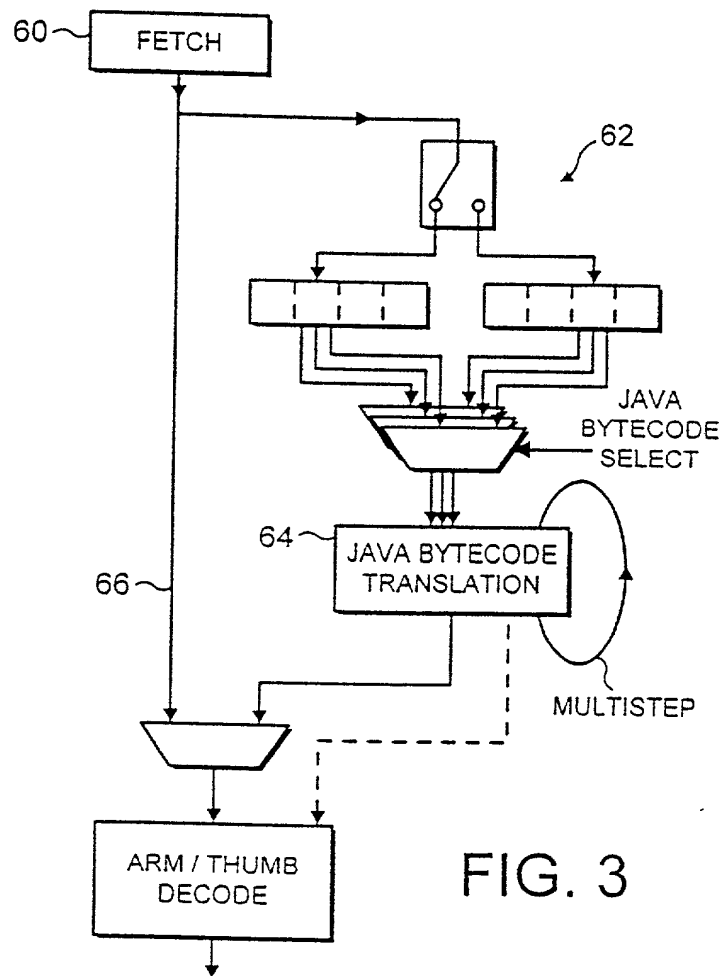


FIG. 3

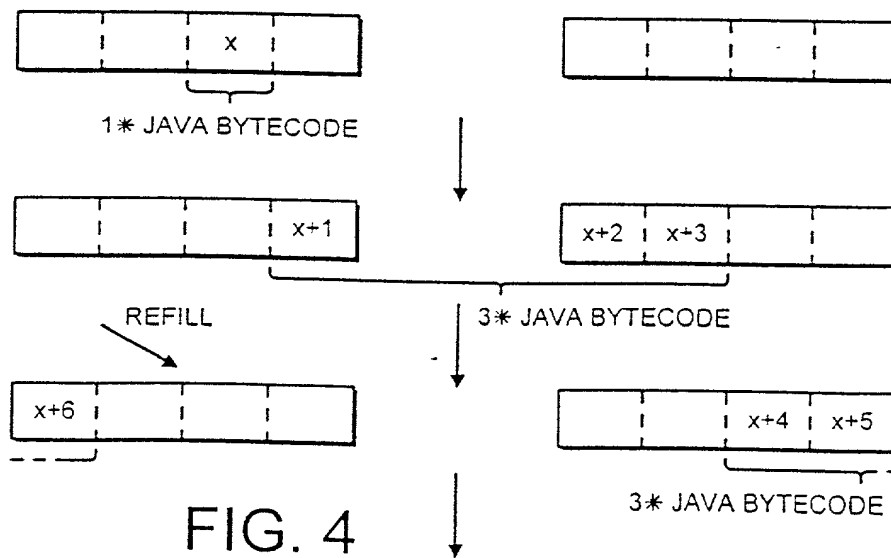


FIG. 4

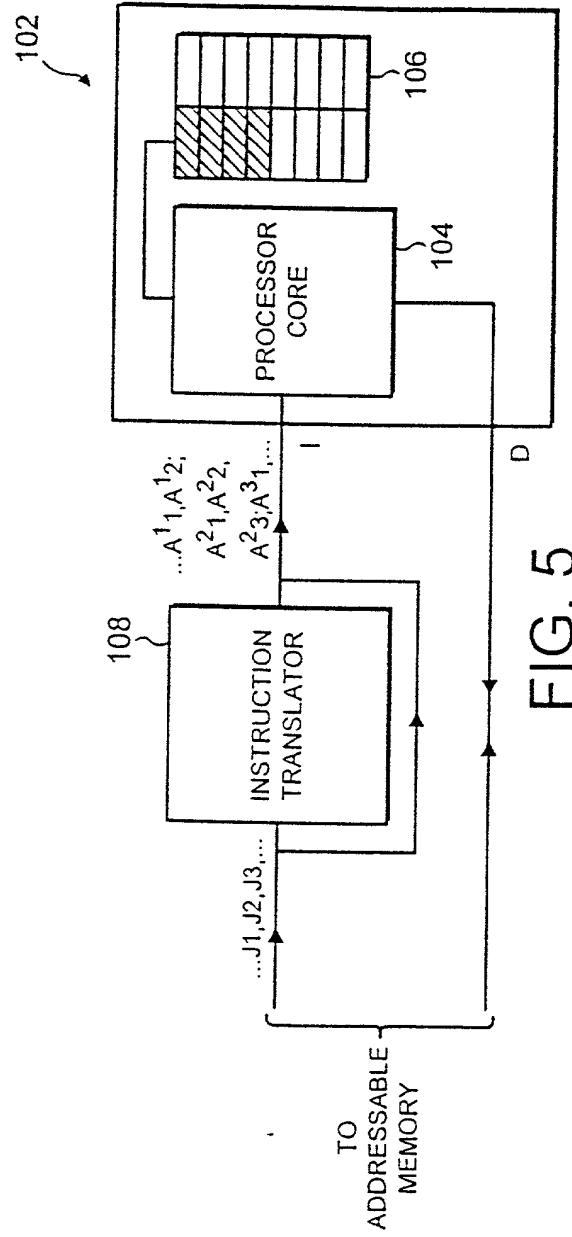


FIG. 5

JAVA INSTRUCTION	iadd (RF=2, RF>0)	iadd (RF=2, RF>1)	iadd (SA=-1)
ARM INSTRUCTION(S)	↗ LDR R0,[RStack,#-4]! (POP) ↗	LDR R3[RStack,#-4]! (POP) ↗	ADD R3, R3, R0 ↗
STATE	00000	00100	01000
R0	E	SOA TOS	SOA TOS
R1	E	E	E
R2	E	E	E
R3	E	E	SOB TOS-1 (SOA+SOB) TOS

	↗ load ¹ (RF=0, RE>2) ↗	↗ load ² (RF=0, RE>2) ↗	↗ load ² (RF=0, RE=2) ↗
JAVA INSTRUCTION			
ARM INSTRUCTIONS	↗ LDR R1,[Rvars,#4] ↗ LDR R0,[Rvars,#0] ↗	↗ STR R3[RStack,#-4] (PUSH) ↗	↗ LDR R3,[Rvars,#4] ↗ LDR R2,[Rvars,#0] ↗
STATE	00000	00100	01000
R0	E	SOC TOS-1	SOC TOS-3
R1	E	SOD TOS	SOD TOS-2
R2	E	E	SOE TOS-1
R3	(SOA+SOB) TOS	(SOA+SOB) TOS	SOF TOS

FIG. 6

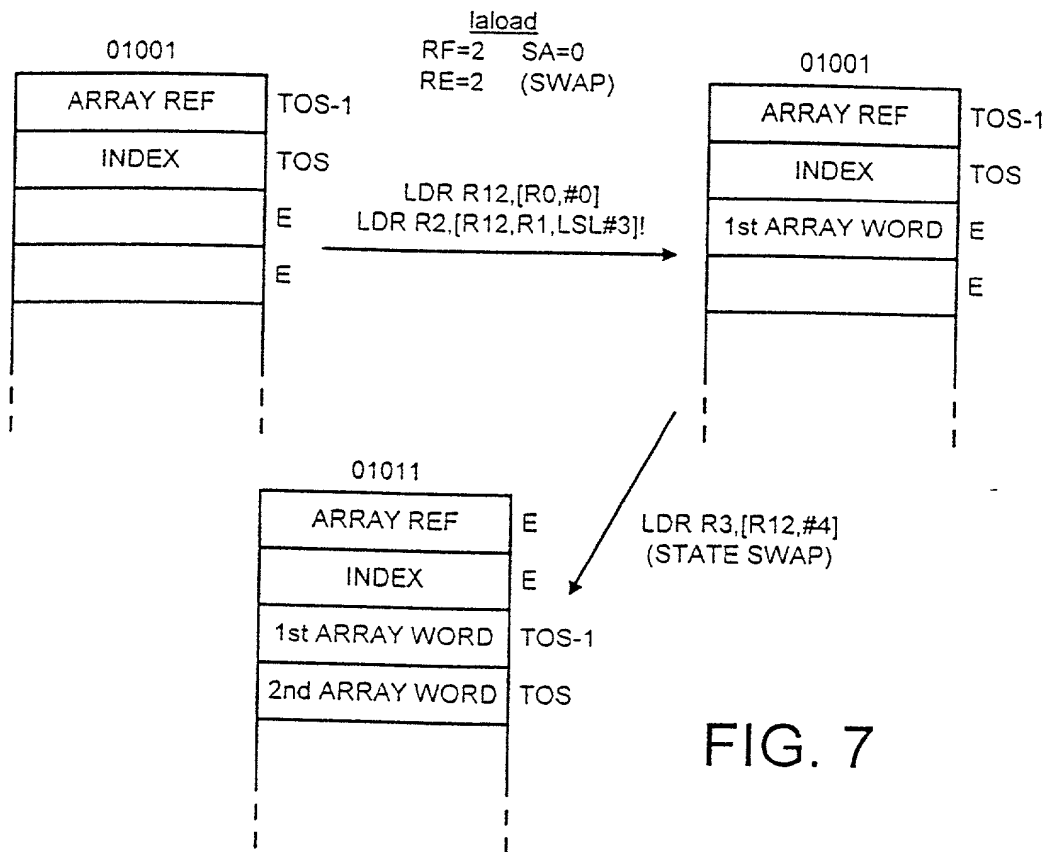


FIG. 7

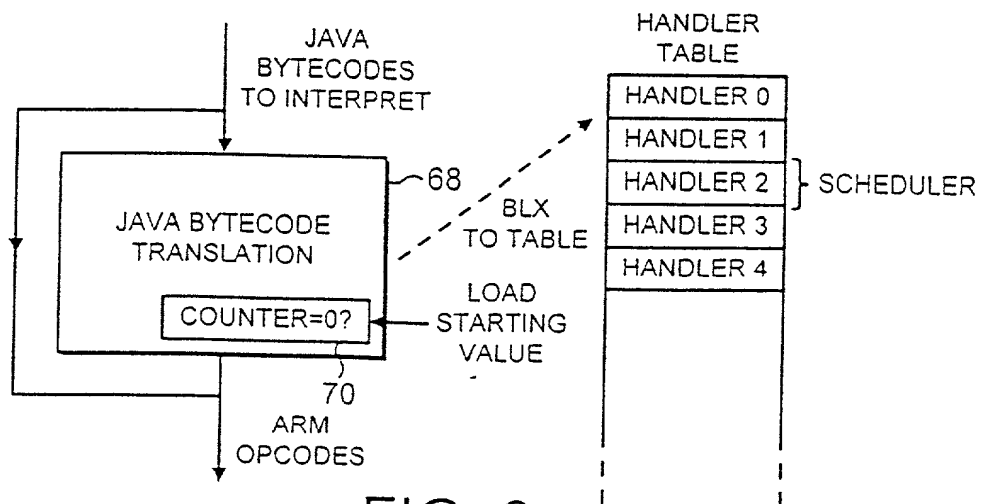


FIG. 9

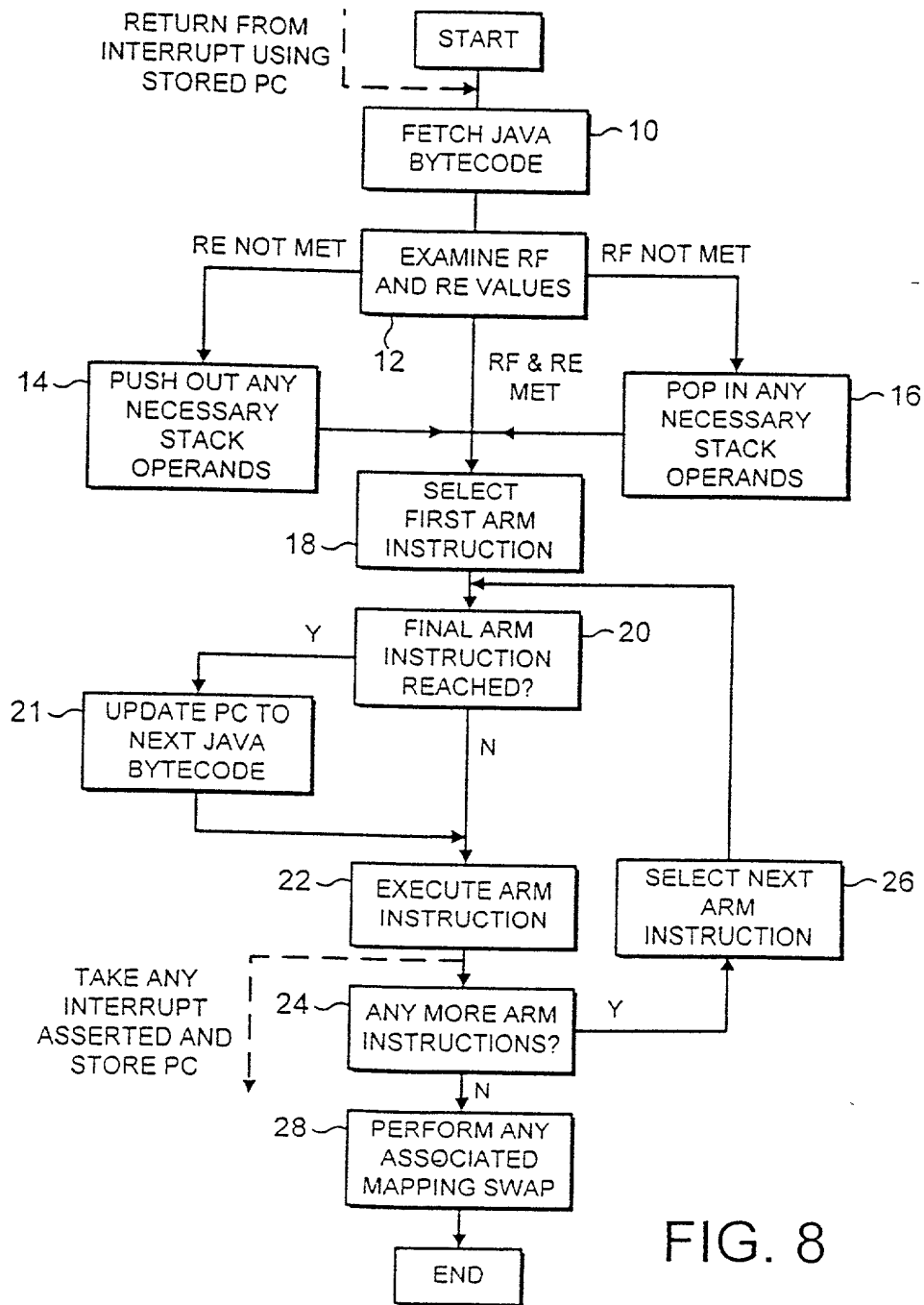


FIG. 8

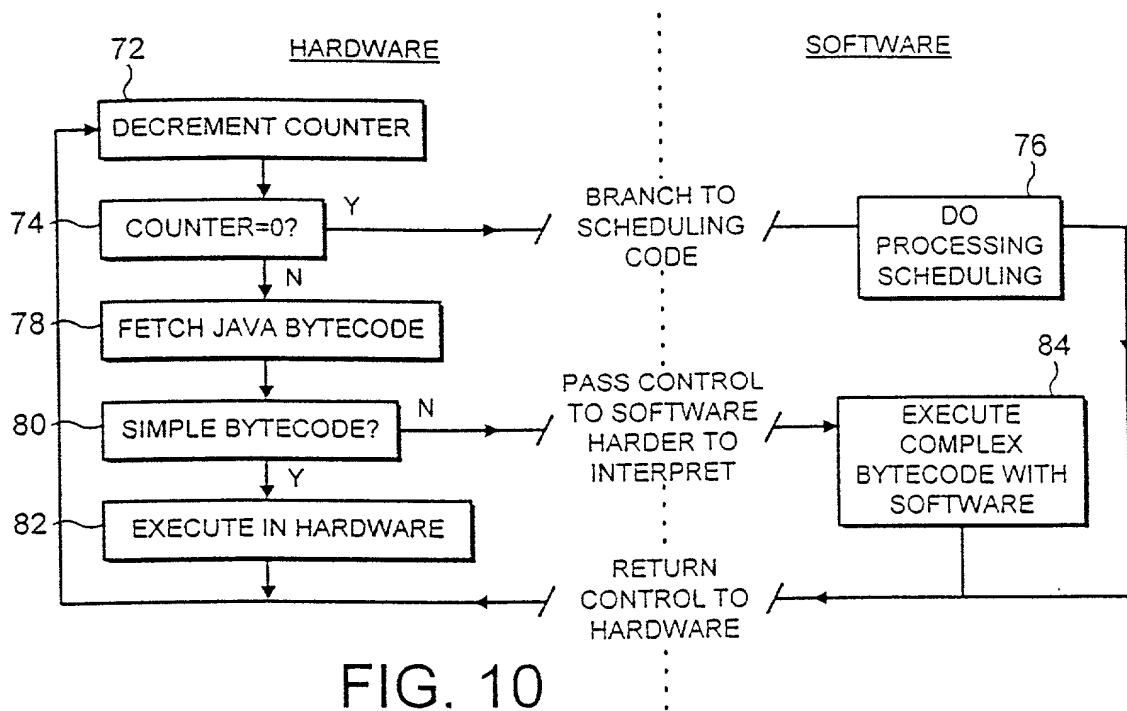


FIG. 10

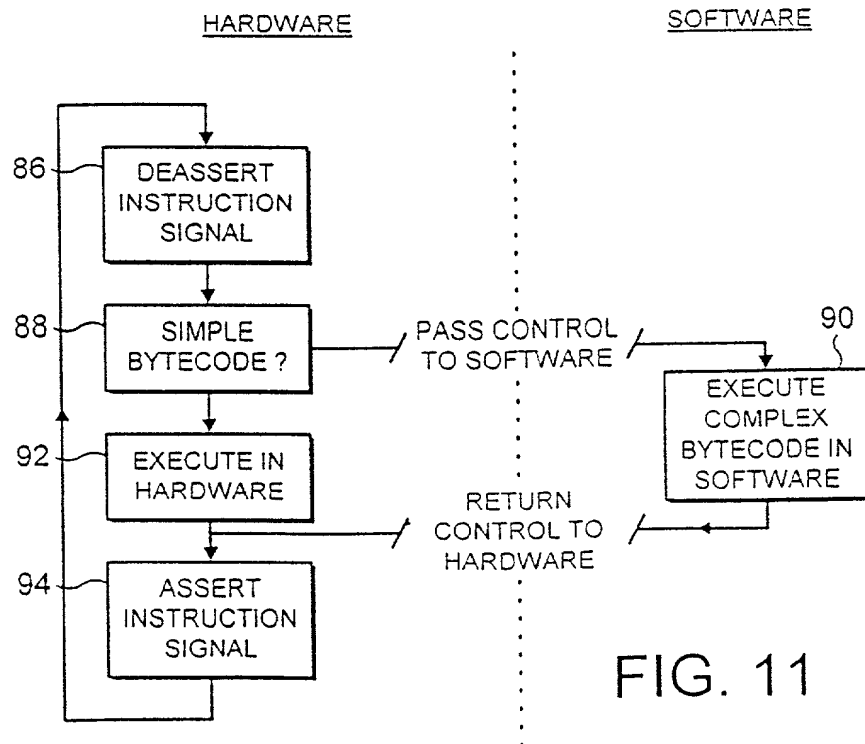


FIG. 11

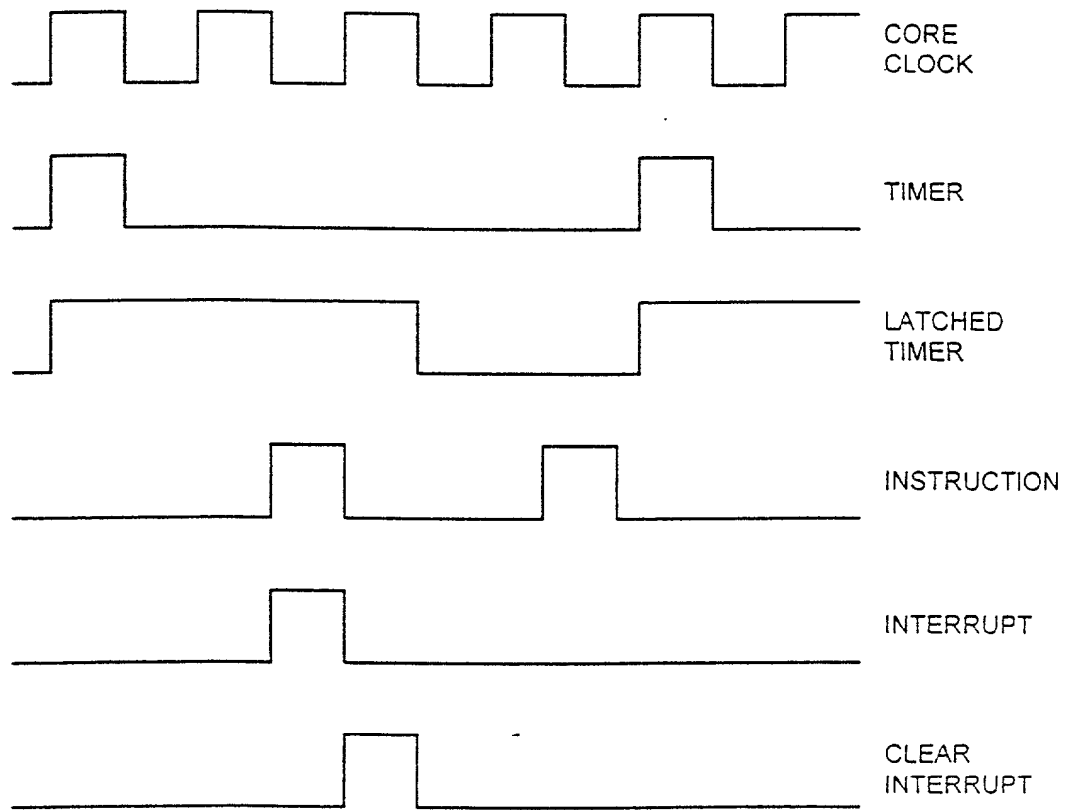
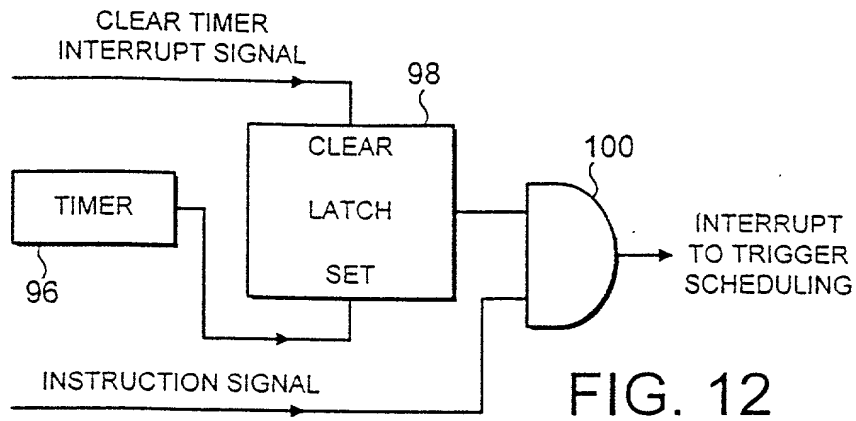


FIG. 13